WHAT IS CLAIMED IS:

1.   A packet switch comprising:

a plurality of line interfaces each connectable to an input line and an output line;

a back panel capable of mounting n crossbar switches each connected to said plurality of line interfaces, each of said plurality of line interfaces including input queue buffers as many as said plurality of line interfaces; a block distributor; and a read controller for reading input packets buffered in said plurality of input buffers, in fixed length block units at cyclic time slots allocated to said n crossbar switches, and sending read blocks to said distributor,

wherein n crossbar switches are mounted on said back panel, said read controller reads n blocks from one input queue buffer selected out of said plurality of input buffers at time slots corresponding to said n crossbar switches, and sends said blocks to said block distributor, wherein said block distributor outputs said n blocks to said n crossbar switches, wherein when k crossbar switches out of said n crossbar switches are unused or faults occur in said k crossbar switches, said read· controller reads n-k blocks from one selected input queue buffer out of said plurality of input queue buffers at time slots corresponding to n-k crossbar switches in operation and sends said blocks to said block distributor but does not read blocks at time slots corresponding to said k crossbar

switches, and wherein said block distributor outputs said n-k blocks to said n-k crossbar switches in operation.

2.   A packet switch according to Claim 1, wherein each line interface of said plurality of line interfaces includes a header inserter, and when n crossbar switches are mounted on said back panel, said block distributor outputs said n blocks each added with a header generated by said header inserter, wherein when k crossbar switches out of said n crossbar switches are unused or when faults occur in said k crossbar switches, said block distributor outputs said n-k blocks each added with a header generated by said header inserter to said n-k crossbar switches in operation, and outputs headers generated by said header inserter to said k crossbar switches.

3.   A packet switch according to Claim 2, wherein each line interface of said plurality of line interfaces includes a header extractor and output queue buffers as many as said plurality of line interfaces, wherein a first identifier is written in headers added to said n blocks and said n-k blocks, and a second identifier is added to headers output to said k crossbar switches, and wherein said header extractor sends only blocks each added with a header having said first identifier written therein, out of data from the n switches, to output queue buffers.

4.   A packet switch comprising:

        a plurality of line interfaces each
connectable to an input line and an output line;

        a back panel capable of mounting n crossbar
switches each connected to said plurality of line
interfaces, each of said plurality of line interfaces
including input queue buffers as many as said plurality
of line interfaces; a block distributor; and a read
controller for reading input packets buffered in said
plurality of input buffers, in fixed length block units
at cyclic time slots allocated to said n crossbar
switches, and sending read blocks to said block
distributor,

        wherein when n-k crossbar switches are
mounted on said back panel, said read controller reads
n-k blocks from one input queue buffer selected out of
said plurality of input buffers at time slots allocated
to said n-k crossbar switches, and sends said blocks to
said block distributor, but does not read blocks at
time slots allocated to k crossbar switches not mounted
on said back panel, wherein said block distribution
controller outputs said n-k blocks to said n-k crossbar
switches, wherein when one crossbar switch is
additionally mounted to said back panel, said read
controller reads n-k+1 blocks from one input queue
buffer selected out of said plurality of input queue
buffers at time slots allocated to said n-k crossbar
switches and also at time slots corresponding to said

additionally mounted crossbar switch, sends said blocks
to said block distributor, and said block distributor
outputs said n-k+1 blocks to said n-k crossbar switches
and said additionally mounted crossbar switch.

5.   A packet switch comprising:

        a plurality of line interfaces each
connectable to an input line and an output line;

        a back panel capable of mounting n crossbar
switches each connected to said plurality of line
interfaces, each of said plurality of line interfaces
including input queue buffers as many as said plurality
of line interfaces; a block distributor; and a read
controller for reading input packets buffered in said
plurality of input buffers, in fixed length block units
at cyclic time slots allocated to said n crossbar
switches, and sending read blocks to said distributor,

        wherein n crossbar switches are in operation
on said back panel, said read controller reads n blocks
from one input queue buffer selected out of said
plurality of input buffers at time slots corresponding
to said n crossbar switches, and sends said blocks to
said block distributor, wherein said block distributor
outputs each of said n blocks to a crossbar switch
corresponding to a time slot at which the block was
read, wherein when k crossbar switches out of said n
crossbar switches are unused or faults occur in said k
crossbar switches, said read controller reads n-k
blocks from one selected input queue buffer out of said

plurality of input queue buffers at time slots
corresponding to n-k crossbar switches in operation and
sends said blocks to said block distributor but does
not read blocks at time slots corresponding to said k
crossbar switches, and wherein said block distributor
outputs said n-k blocks to crossbar switches
corresponding to time slots at which said blocks were
read.

6.   A packet switch according to Claim 5, wherein
said read controller reads input packets buffered in
said plurality of input queue buffers, in fixed length
block units starting from head of each queue at cyclic
time slots allocated to said n crossbar switches.

7.   A packet switch according to Claim 5, wherein
when each line interface of said plurality of line
interfaces includes a header inserter and n crossbar
switches are mounted on said back panel, said block
distributor outputs said n blocks each added with a
header generated by said header inserter, wherein when
k crossbar switches out of said n crossbar switches are
unused or faults occur in said k crossbar switches,
said block distributor outputs said n-k blocks each
added with a header generated by said header inserter,
and outputs headers generated by said header inserter
to said k crossbar switches.

8.   A packet switch according to Claim 6, wherein
each line interface of said plurality of line
interfaces includes a header inserter and n crossbar

switches are mounted on said back panel, said block
distributor outputs said n blocks each added with a
header generated by said header inserter, wherein when
k crossbar switches out of said n crossbar switches are
unused or faults occur in said k crossbar switches,
said block distributor outputs said n-k blocks each
added with a header generated by said header generator,
and outputs headers generated by said header generator
to said k crossbar switches.

9.   A packet switch according to Claim 7, wherein
each line interface of said plurality of line
interfaces includes a header extractor and output queue
buffers as many as said plurality of line interfaces,
wherein a first identifier is written in headers added
to said n blocks and said n-k blocks and a second
identifier is written in headers outputs from said k
crossbar switches, and wherein said header extractor
outputs only blocks added with headers having said
first identifier written therein, out of data from said
n switches, to output queue buffers.

10.   A packet switch according to Claim 8, wherein
each line interface of said plurality of line
interfaces includes a header extractor and output queue
buffers as many as said plurality of line interfaces,
wherein a first identifier is written in headers added
to said n blocks and said n-k blocks and a second
identifier is written in headers output from said k
crossbar switches, and wherein said header extractor

outputs only blocks added with headers having said first identifier written therein, out of data sent from said n switches, to said output queue buffers.